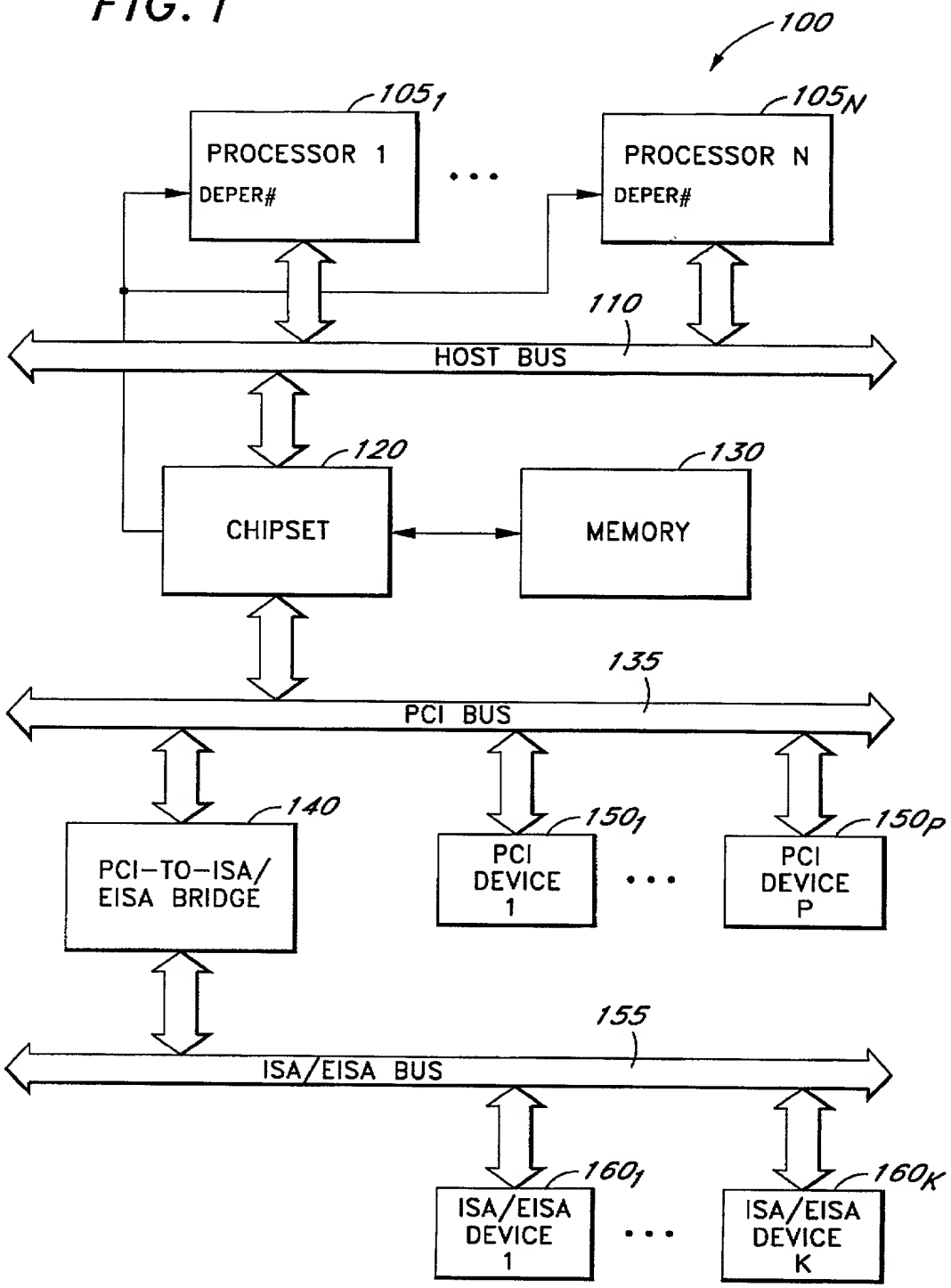
FIG. 1


100
105₁
PROCESSOR 1
DEPER#
105N
PROCESSOR N
DEPER#
110
HOST BUS
120
CHIPSET
130
MEMORY
135
PCI BUS
140
PCI-TO-ISA/
EISA BRIDGE
150₁
PCI
DEVICE
1
150P
PCI
DEVICE
P
155
ISA/EISA BUS
160₁
ISA/EISA
DEVICE
1
160K
ISA/EISA
DEVICE
K

SNOOP RESULT	COMPLETE	NEXT ORERED	HIT#	HITM#	DEFER#	VSBL#
CLEAN	YES	ALLOWED	INACTIVE	INACTIVE	INACTIVE	X
SHARED	YES	ALLOWED	ACTIVE	INACTIVE	INACTIVE	X
MODIFIED	YES	ALLOWED	INACTIVE	ACTIVE	X	X
STALL	NO	WAIT	ACTIVE	ACTIVE	X	X
DEFERERD	NO	WAIT	X	INACTIVE	ACTIVE	INACTIVE
	NO	ALLOWED	X	INACTIVE	ACTIVE	ACTIVE

FIG. 2

FIG. 3

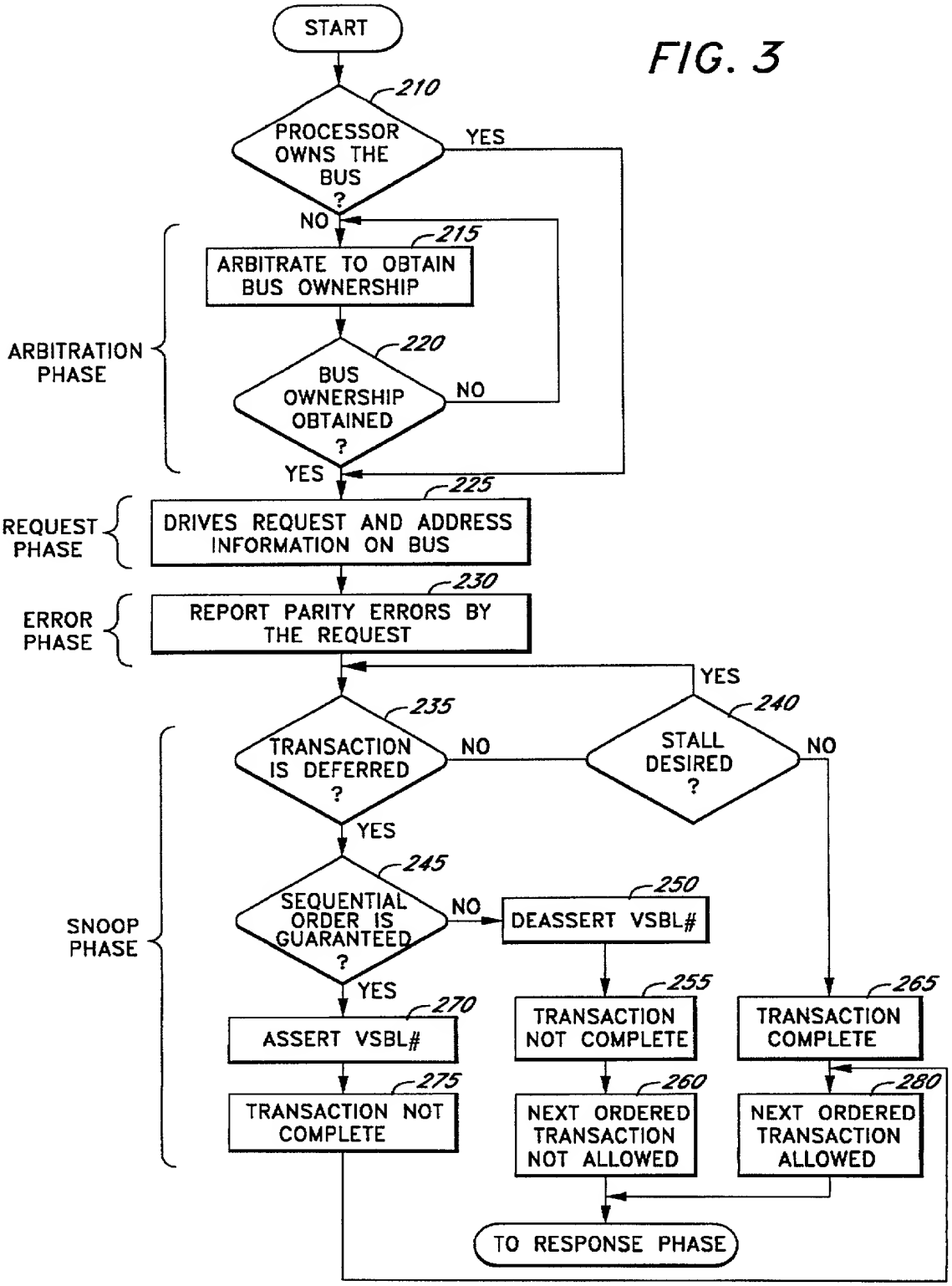
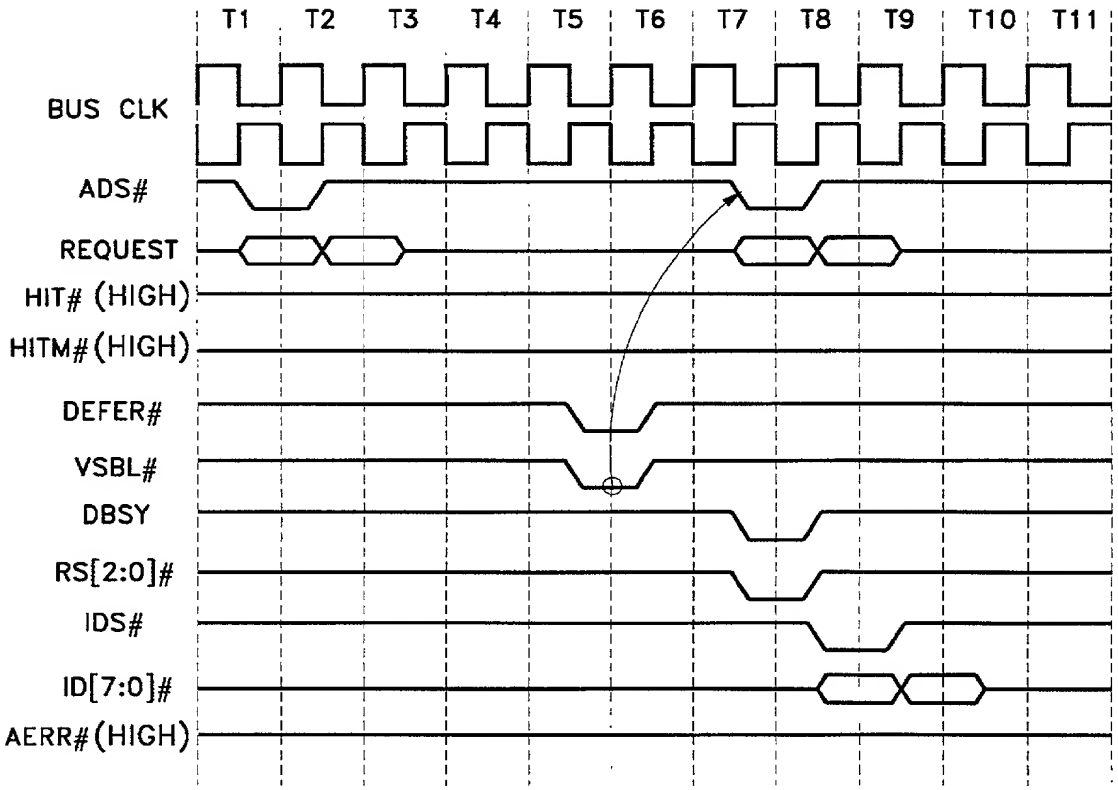

START
210
PROCESSOR OWNS THE BUS ?
YES
NO
215
ARBITRATE TO OBTAIN BUS OWNERSHIP
220
BUS OWNERSHIP OBTAINED ?
NO
YES
ARBITRATION PHASE
225
DRIVES REQUEST AND ADDRESS INFORMATION ON BUS
REQUEST PHASE
230
REPORT PARITY ERRORS BY THE REQUEST
ERROR PHASE
YES
235
TRANSACTION IS DEFERRED ?
NO
240
STALL DESIRED ?
NO
YES
245
SEQUENTIAL ORDER IS GUARANTEED ?
NO
250
DEASSERT VSBL#
YES
270
ASSERT VSBL#
275
TRANSACTION NOT COMPLETE
255
TRANSACTION NOT COMPLETE
260
NEXT ORDERED TRANSACTION NOT ALLOWED
265
TRANSACTION COMPLETE
280
NEXT ORDERED TRANSACTION ALLOWED
SNOOP PHASE
TO RESPONSE PHASE

FIG. 4


T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
BUS CLK
ADS#
REQUEST
HIT# (HIGH)
HITM# (HIGH)
DEFER#
VSBL#
DBSY
RS[2:0]#
IDS#
ID[7:0]#
AERR# (HIGH)